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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/742,036

12/20/2000

Toshiyuki Matsuzaki

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TEXAS INSTRUMENTS INCORPORATED

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EXAMINER

SHAPIRO, LEONID

ART UNIT

PAPER NUMBER

2673

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/742,036

Applicant(s)

MATSUZAKI, TOSHIYUKI

Examiner

Leonid Shapiro

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 1899.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 1-10, 12, 20 and 23 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14-19 and 21 is/are allowed.
- 6) ☒ Claim(s) 11, 13, 22, 24-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 11, 22, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cha et al. (US Patent No. 6,519,020 B1) in view of Mical et al. (US Patent No. 6,191,772 B1) and Chen (US Patent No. 6,456,353 B1).

As to claim 11, Cha et al. teaches a module for a display device comprising:

a wiring substrate (See Figs. 3, 5 item 62, 92, in description See Col. 5, Lines 27-31 and from Col. 5, Line 66 to Col. 6, Line 1),

a plurality of integrated circuits mounted on the wiring substrate, each integrated circuit having inputs coupled to n input terminals (where n is a natural number and $n \geq 2$) to receive a data signals (See Fig. 5, items 92, 94, 106, in description See Col. 6, Lines 1-27), each of the integrated circuits having the inputs arranged linearly in a row along a first side and the output on a second side parallel to the first side, the second side facing the display device, the first side facing away from the display device (See Fig. 5, items 92, 94, 106, in description See Col. 6, Lines 1-27).

Cha et al. does not teach the single level of wiring on wiring substrate connected to the n input terminals to couple data signals are being parallel lines.

Chen teaches the single level of wiring (See Fig. 5, items 506) on wiring substrate (See Fig. 5, items 504) connected to the n input terminals (See Fig. 5, items 508) to couple data signals are being parallel lines (See Fig. 5, items 502, 504, 506, Col. 4, Lines 13-31).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement Chen approach in the Cha et al. apparatus in order to reduce cost, size and thickness (See Col. 2, Lines 45-54 in Chen reference).

Cha et al. and Chen do not teach switching circuit generating n output signals coupled to a drive signal generation circuit for driving the display device, the switching circuit sequentially connects first through n -th input terminals to first through n -th output terminals respectively when a control signal is at the first logical level and sequentially connects first through n -th input terminals to first through m -th output terminals respectively when a control signal is at the second logical level.

Mical et al. teaches cross-over unit which can place appropriate even or odd-numbered pixel signals on respective side buses (See Fig. 1, items 150, 151, 154, in description See Col. 13, Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement Mical et al. approach in the Cha et al. and Chen apparatus applying it to first through n -th input terminals to first through n -th output terminals respectively in order to reduce the number of parts (See Col. 3, Lines 51-54 in Mical et al. reference).

As to claim 22, Mical et al., Cha et al. and Chen do not show control signal coupled to the plurality of integrated circuits is at the first logic level for one integrated circuit of a pair of integrated circuits and is at second logic level for another integrated circuit of the pair.

Since even and odd drivers connected in series (See Figs. 1-2, items LR#0, LR#2, LR#1, LR#3, Col. 10, Lines 44-56 in Mica et al. reference), it would have been obvious to one of ordinary skill in the art at the time of invention to use the first logic level for one integrated circuit of a pair and second logic level for another integrated circuit of the pair in the Cha et al., Mical et al. and Chen apparatus in order to reduce the number of parts (See Col. 3, Lines 51-54 in Mical et al. reference).

As to claim 25, Chen teaches the wiring for the first integrated circuit approaches the integrated circuit on the wiring substrate from a first direction (See Fig. 5, item 508, Col. 4, Lines 12-32) and the wiring for the second integrated circuit approaches the integrated circuit on the wiring substrate from a second direction opposite to the first direction (See Fig. 5, item 506, Col. 4, Lines 12-32 and Fig. 6b, item 606b, Col. 4, Lines 57-68).

2. Claim 13, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Cha et al. and Mical et al. as aforementioned in claims 11, and 22 in view of Voisin et al. (US Patent No. 5, 680, 191).

Sasaki et al., Cha et al. and Mical et al. do not show the first substrate is a flexible substrate.

Voisin et al. teaches the first substrate is a flexible substrate (See Figs. 3-4, item 50, in description See Col. 11, Lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement approach as shown by Voisin et al. in Chen, Cha et al. and Mical et al. apparatus.

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Cha et al. and Mical et al. as aforementioned in claim 22 in view of Udo et al. (US Patent No. 6,304,241 B1).

Chen, Cha et al. and Mical et al. do not show the wiring between input terminals and switching circuit comprise a continuous line between a first terminal, an input to the switching circuit and a second terminal.

Udo et al. teaches the a continuous line between a first terminal, an input to the switching circuit and a second terminal (See Fig. 25, items Ma1, Mb1, 352, Col. 18, Lines 56-65).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Udo et al. in Chen, Cha et al. and Mical et al. system in order to simplify manufacturing process, reduce the production cost.

Allowable Subject Matter

4. Claims 14-19, 21 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Relative to claims 14, 18-19, 21 the major difference between the teaching of the prior art of record (Cha et al., Mical et al. and Chen) and the instant invention is that the said prior art **does not teach** the wiring for the first integrated circuit approaches the integrated circuit on the wiring substrate from a first direction and a wiring for the second integrated circuit approaches the integrated circuit on the wiring substrate from a second direction opposite to the first direction.

Relative to claims 15-17 the major difference between the teaching of the prior art of record (Cha et al., Mical et al. and Chen) and the instant invention is that the said prior art **does not teach** wiring between the n-input terminals and the switching circuit comprise a continuous line between a first terminal, an input to the switching circuit and a second input terminal.

Response to Arguments

6. In response to applicant's argument on page 9, 1st paragraph of Remarks that Mica et al. is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Mica et al. reference is reasonably pertinent to the particular problem with which the applicant was concerned.

Response to Amendment

7. Applicant's arguments filed on 10-04-04 with respect to claims 11, 13-22, 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

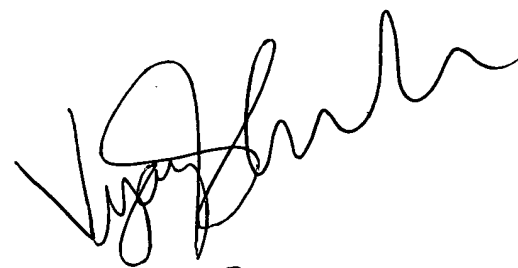
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls

01.04.04



VIJAY SHANKAR
PRIMARY EXAMINER